ERSA: Error Resilient System Architecture
For Probabilistic Applications

Hyungmin Cho, Subhasish Mitra

**Motivation**
Recognition, Mining, Synthesis (RMS) : Killer Applications
Massive amount of computation loads

Unique Opportunity:
- Error resiliency
- Probabilistic computation
- Iterative convergence
- Cognitive resilience: Acceptable results are OK

RMS on unreliable hardware: DOESN'T WORK
- Frequent crash / Highly inaccurate result

**Error Resilient System Architecture**

**Error Injection Techniques**

Importance of low-level error injection:
- Low-level (Flip-flop) vs. High-Level (Arch. Registers)

Error injection to various layers:
- Low-level flip-flop
- Architectural register file
- Memory error injection

Flexible injection:
- Various rate
- Pattern / Interval

ERSA Prototype Error Injection

SRAM V_{ccmin} Challenge

- Huge Power Saving
- Persistent Errors (Variation-induced)

ERSA solution:
- Offset shifting cache
- Pseudo-random effect
- Low H/W overhead

**ERSA + Stochastic Computing**

Enhanced ERSA:
- Basic ERSA + Algorithmic Enhancements
- High error-resilience

Limitation: Based on Heuristic Rules
- Programming effort
- Result may not be optimal

Systematic methods required!

**Future Plan**
Many collaborative opportunities:
- Ex) intelligent task scheduling with information theory
- LDPC Gallager B decoder modeling
  Prof. Lara Dolecek @ UCLA

Application opportunities:
- Medical applications
- Graphic applications

**ERSA Prototype on FPGA**
BEE3 system
- Virtex-5 FPGAs
- 16GB DRAM
- LEON3 cores
- 1 SRC, 8 RRCs

**ERSA Emulation Results**

K-Means Clustering
LDPC Decoding
Bayesian Network Inference

**SRAM Error Injection Results**

ERSA + Stochastic Computing

DCT Application

PSNR (dB)

Future Plan

Many collaborative opportunities:
- Ex) intelligent task scheduling with information theory
- LDPC Gallager B decoder modeling
  Prof. Lara Dolecek @ UCLA

Application opportunities:
- Medical applications
- Graphic applications