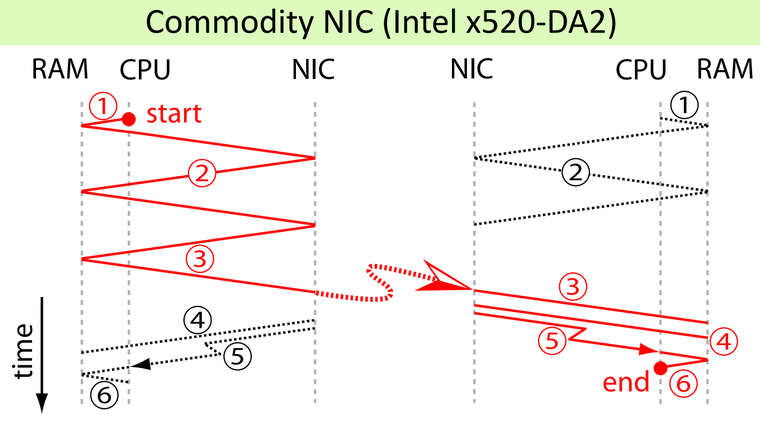
Authors: Mario Flajslik, Mendel Rosenblum

Title: Network Interface Design for Low Latency Request-Response Protocols

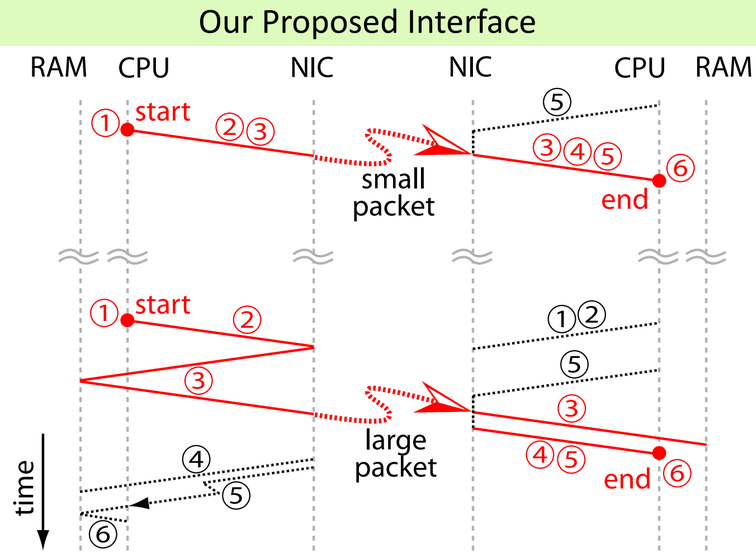
Motivation

Commodity NIC (Intel x520-DA2)



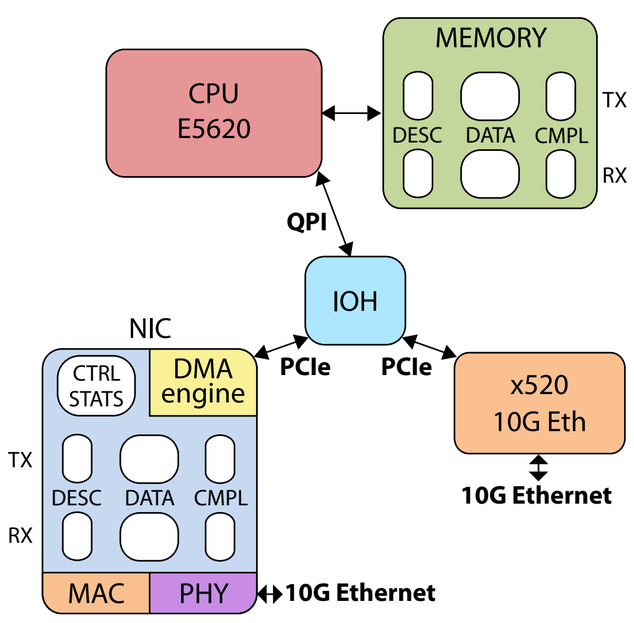
Multiple PCIe round-trips and transitions are the main source of latency for all packets.

Our Proposed Interface

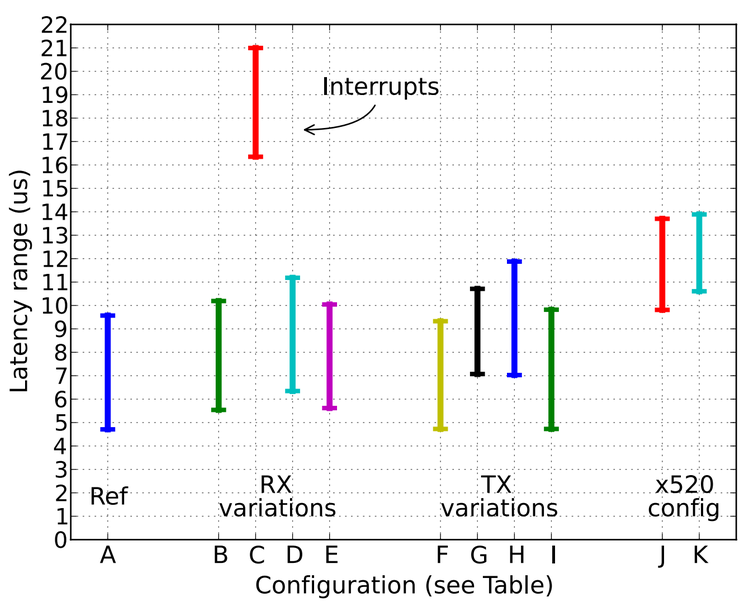


Network Interface Design

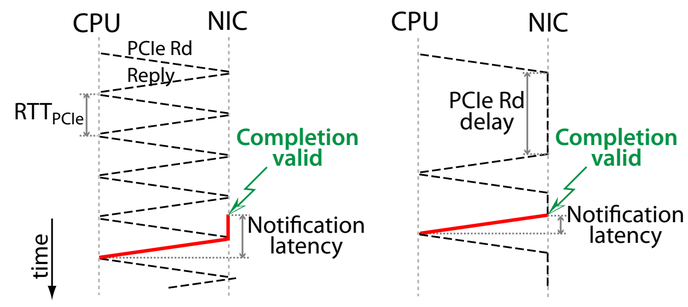
System Diagram



Configuration comparison



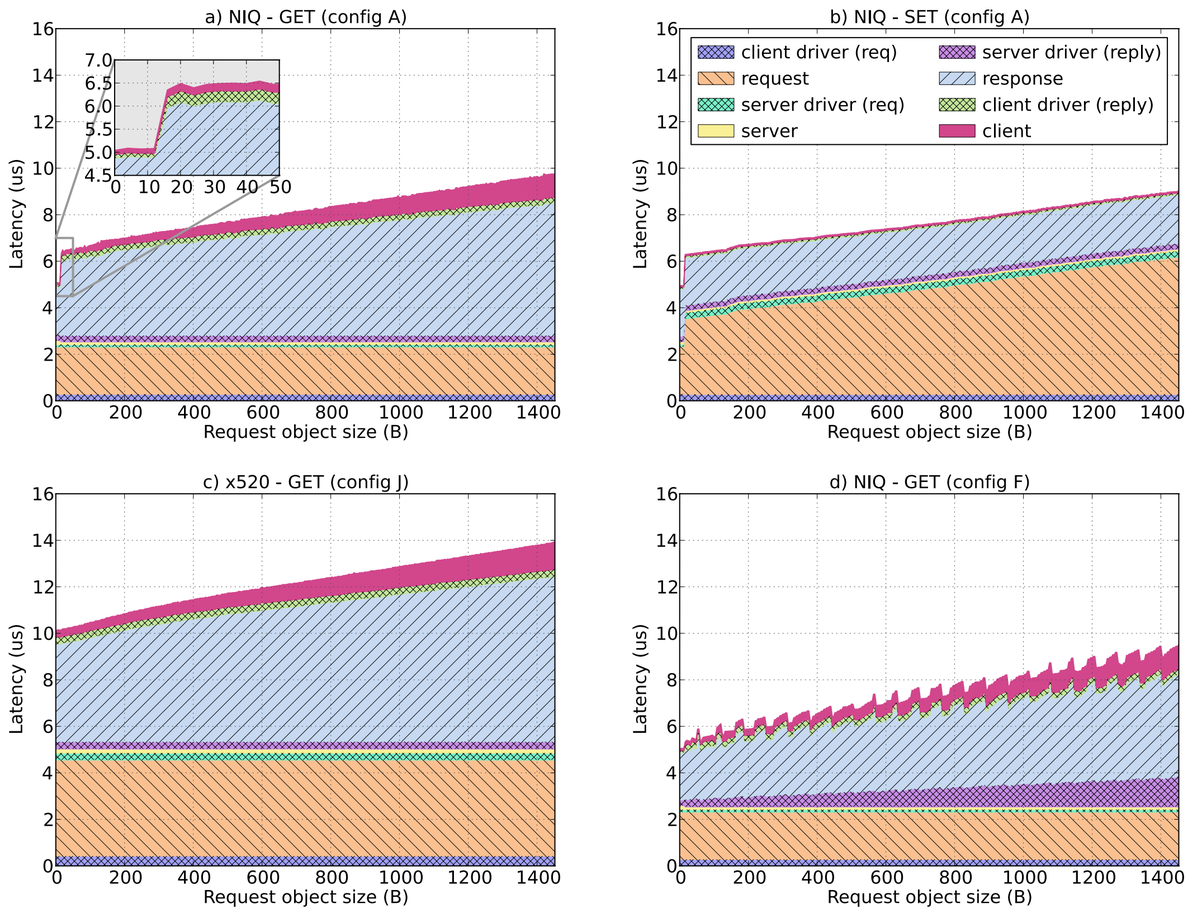
Custom polling



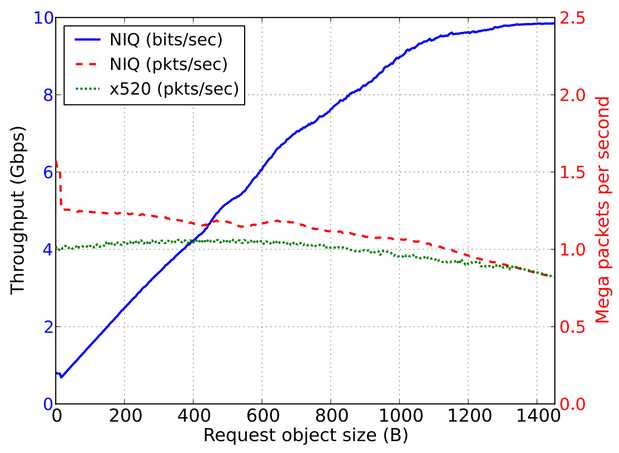
		A	B	C	D	E	F	G	H	I	J	K
NIC	NIQ	•	•	•	•	•	•	•	•	•		•
	x520										•	
RX	small pkt	•	•	•	•		•	•	•	•		
	niq poll	•				•	•	•	•	•		
	host poll		•								•	•
	interrupt			•								
	mwait				•							
TX	small pkt	•	•	•	•	•	•		•	•		
	hdr split	•	•	•	•	•	•	•	•		•	•
	no DMA						•					
	doorbell								•		•	•

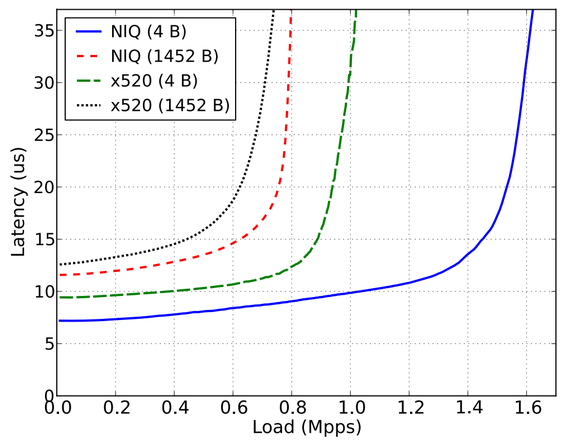
Evaluation

Latency breakdown

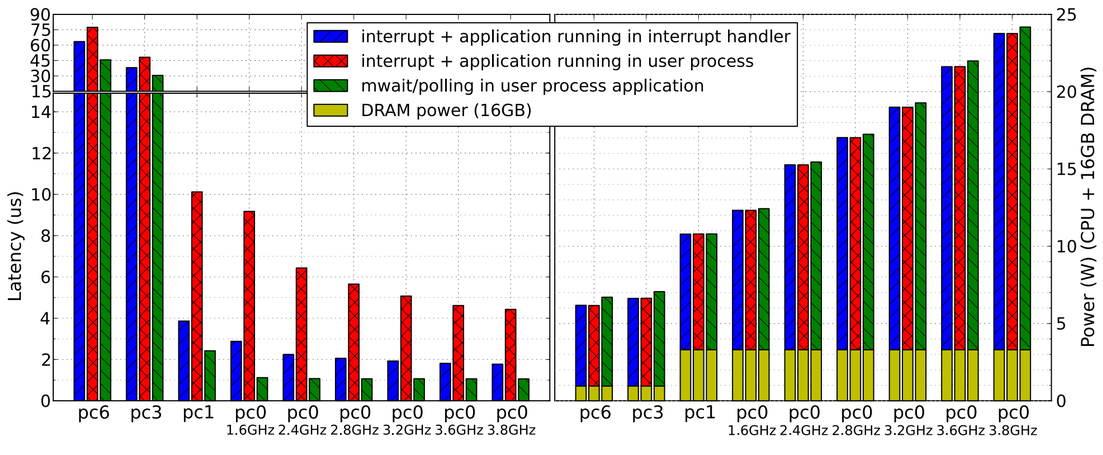


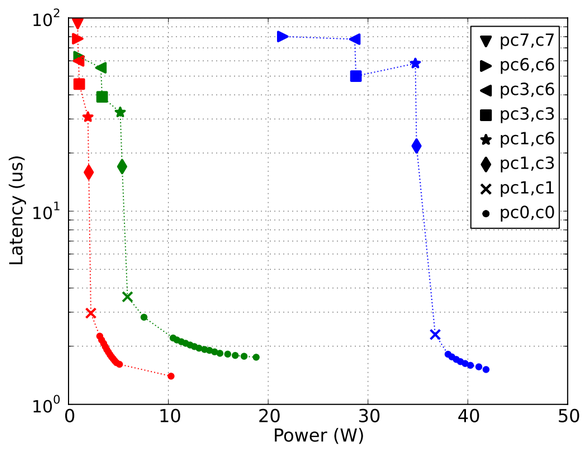
Bandwidth





Power Analysis





Conclusion: We demonstrate 2X latency improvements by focusing on minimizing the number of transitions over the PCIe interconnect, particularly for small packets. Moreover, we infer a possibility for another 2X latency gain (overall 4X gain) by implementing our system on state of the art components.