Quick Error Detection for Effective Post-Silicon Validation

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**Long Error Detection Latency**
- Test execution: Error occurred
- Error detected: Error detection latency
  - Ideal: ~ 1,000 cycles
  - Reality: ~ Billions cycles

**Localization Domination Cost**
- Run tests: Detect bugs
- Debug time: 1-4 weeks per bug
- Root-cause & fix: Localize bugs

**Quick Error Detection**
- Original Tests
  - Test 1
  - Test 2
  - ...
  - Test N
- QED Core + Uncore Transformation Example
- QED Tests
  - QED Test 1
  - QED Test 2
  - ...
  - QED Test N

**Wide variety**
- Diversity
- Systematic, structured, automated
- Error detection latency: 10^6X improved
- Coverage: 4X improved
- Software only: readily application

**Key challenge:** Long error detection latency

**New technique:** Quick Error Detection
- Systematic, structured, automated
- Error detection latency: 10^6X improved
- Coverage: 4X improved
- Software only: readily application

**Intel® Core i7™ Hardware**
- QED
- No-QED
- Detected error count (normalized to QED)
- Error detection latency (clock cycles)
- 0-10K
- 1-10 Billion

**QED Core + Uncore Transformation Example**

**Localization**

**8 Cores LU Test from Splash2**
- Original
- 10^4X
- 2X
- Cumulative bug detected

**8 Cores FFT Test from Splash2**
- Original
- 10^4X
- 2X
- Cumulative memory bugs detected

**8 Cores Industrial Validation Test**
- Original
- 10^6X
- Improved
- Cumulative memory bugs detected